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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/803,190	03/18/2004	Shunpei Yamazaki	0756-7269	5109

31780 7590 07/24/2008

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EXAMINER	
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ART UNIT	PAPER NUMBER
2629	

MAIL DATE	DELIVERY MODE
07/24/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/803,190	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	MY-CHAU T. TRAN	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 May 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) *2-5,8,9,12,13 and 15-22* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,6,7,10,11,14 and 23-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 05/23/2008 has been entered.

Application and Claims Status

2. Applicant's amendment and response filed 04/23/2008 are acknowledged and entered.

3. Claims 1-31 were pending. Applicants have amended claims 1, 7, 11, and 23-25. No claims were added and/or cancelled. Therefore, claims 1-31 are currently pending. Claims 2-5, 8, 9, 12, 13, and 15-22 are drawn to non-elected species and/or inventions and thus these claims remain withdrawn from further consideration by the examiner, 37 CFR 1.142(b), there being no allowable generic claim. Accordingly, claims 1, 6, 7, 10, 11, 14, and 23-31 are under consideration in this Office Action.

Status of Claim(s) Objection(s) and /or Rejection(s)

4. All previous claims objection(s) and/or rejection(s) have been withdrawn in view applicant's amendments of claims 1, 7, 11, and 23-25 thereto, specifically the added limitation of

'*wherein a semiconductor layer of the first transistor continues to a semiconductor layer of the second transistor*'.

5. The provisionally rejection under the judicially created doctrine of obviousness-type double patenting of claims 23 and 24 over claims 3, 4, 7, 8, 11, 12, 15, and 16 of copending Application No. 11/208,278 (US Patent Application Publication 2006/0044229 A1) has been withdrawn in view of applicant's amendments of claims 1, 7, 11, and 23-25, specifically the added limitation of '*wherein a semiconductor layer of the first transistor continues to a semiconductor layer of the second transistor*'.

New Rejection(s) – Necessitated by Amendment

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later

invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 1, 6, 7, 10, 11, 14, and 23-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishitoba et al. (US Patent 6,774,877) in view of Yudasaka (US Patent 6,359,606 B1).

For ***claims 1, 6, 7, 10, 11, 14, and 23-31***, Nishitoba et al. disclose an organic electroluminescent (EL) image display device (see e.g. Abstract; col. 1, lines 7-12; col. 3, line 49 thru col. 4, line 14; fig. 3). As illustrated by figure 3, the device comprises an organic EL element (ref. #11) (refers to instant claimed light emitting element/pixel electrode) and two transistors (ref. #8 and 9) (refers to instant claimed first and second transistors) connected to the organic EL element in a series (see e.g. col. 6, lines 17-59). The anode of the organic EL element (ref. #11) is connected to the drain (refers to instant claimed limitation of '*one of a source region and a drain region of the first transistor is connected to the light emitting element*') of transistor (ref. #8)(refers to instant claimed first transistor) and the source of transistor (ref. #8) is connected to the drain of transistor (ref. #9)(refers to instant claimed second transistor) (refers to instant claimed limitation of '*the other one of the source region and the drain of the first transistor is connected to one of a source re(lion and a drain region of the second transistor*') (see e.g. col. 6, lines 17-27; fig. 3). Additionally as illustrated by figure 3, the device comprise a switching transistor (ref. #12) (refers to instant claimed third transistor) wherein the drain (refers to instant claimed first electrode of the third transistor) is connected to the signal line (ref. #3) and the source (refers to instant claimed second electrode of the third transistor) is connected to the gate electrodes of both transistors (ref. #8 and 9) (see e.g. col. 6,

lines 28-36). The gates of the transistors (ref. #8 and 9) are connected to each others (refers to instant claimed gate electrodes) and they are p-channel MOS transistors (refers to instant claimed p-type transistor/same polarity) (see e.g. col. 6, lines 24-25 and 39-40; fig. 3). Nishitoba et al. disclose that the transistor (ref. #9) compensates the variations in the threshold voltage of the transistor (ref. #8) (see e.g. col. 6, lines 38-59). The transistor (ref. #8) operates in the saturation region, and the transistor (ref. #9) operates in the non-saturation region, i.e. linear region (see e.g. col. 6, lines 38-59). Nishitoba et al. also disclose that the channel width of transistors of references #6 to #9 is 4 μm, i.e. constant (see e.g. col. 7, lines 42-44). As shown in figure 6, there is a relationship between the channel length of transistors of references #7 and #9 and the variations in output current such that the desired characteristics can be obtained by selecting the channel length of transistors of references #7 and #9 according to the picture quality that is demanded of the image display device (see e.g. col. 6, lines 38-59; col. 7, lines 23-57), which imply that the size of the transistor's channel, i.e. length and width, would be a choice of experimental design and is considered within the purview of the cited prior art. Moreover, Nishitoba et al. disclose that the channel length of transistors of references #7 and #9 can be set to at least 0.5 times or at least one time but not greater than four times the channel length of transistors of references #6 and #8, i.e. if the channel length of transistor (ref. #9) is set at 15 μm then the channel length of transistor (ref. #8) is 7.5 μm such that the channel length of transistor (ref. #9) is 0.5 times that of the channel length of transistor (ref. #8) (see e.g. col. 7, lines 54-57).

For ***claims 11, and 25***, Nishitoba et al. disclose the method of driving the light emitting device wherein the step comprises controlling the current to be supplied to a light emitting device by the first and second transistors (see e.g. col. 3, line 49 thru col. 4, line 14; col. 6, line

60 thru col. 7, line 22; figs. 3 and 4). Moreover, Nishitoba et al. disclose the claimed structural features of the instant claimed light emitting device as discussed above.

The teachings of Nishitoba et al. differ from the presently claimed invention as follows:

For ***claims 1, 7, 11, and 23-25***, Nishitoba et al. fail to disclose the limitation that '*wherein a semiconductor layer of the first transistor continues to a semiconductor layer of the second transistor*', i.e. the first and second transistors are formed on the same substrate/semiconductor layer.

However, Yudasaka teach the limitations that are deficient in Nishitoba et al. as follows:

For ***claims 1, 7, 11, and 23-25***, Yudasaka disclose an active matrix display device and the method of making the device (see e.g. Abstract; col. 1, lines 5-12; col. 2, line 56 thru col. 3, line 7; col. 9, line 1 thru col. 10, line 56). The active matrix device comprises at least two thin film transistors (TFT) and an electroluminescent element (EL element) (see e.g. col. 1, lines 5-12; col. 4, line 59 thru col. 5, line 67; col. 9, lines 2-15; figs. 1-3). As illustrated by figure 3A and 3B, the first TFT (ref. #20) and the second TFT (ref. #30) on the same semiconductor film (see e.g. col. 5, lines 31-45; col. 9, lines 29-54; fig. 2). Both the first TFT (ref. #20) and the second TFT (ref. #30) can be P-type transistor (see e.g. col. 10, lines 46-56).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to disclose that the first and second transistors are formed on the same substrate/semiconductor layer as taught by Yudasaka in the device of Nishitoba et al. One of ordinary skill in the art would have been motivated to the first and second transistors are formed on the same substrate/semiconductor layer in the device of Nishitoba et al. for the advantage of providing an active matrix display device employing an electroluminescent element in which no

opposing substrate is required (Yudasaka: col. 11, lines 24-54). Additionally, both Nishitoba et al. and Yudasaka disclose an active matrix device comprises at least two thin film transistors and an electroluminescent element (Nishitoba: fig. 3; Yudasaka: fig. 1). Furthermore, one of ordinary skill in the art would have a reasonable expectation of success in the combination of Nishitoba et al. and Yudasaka because Yudasaka disclose that the method for forming the TFT does not require any modification of the well-known process (see e.g. col. 10, lines 46-56), and as a result forming the transistors on the same substrate/semiconductor layer would be a choice of experimental design and is considered within the purview of the cited prior art.

Therefore, the combine teachings of Nishitoba et al. and Yudasaka do render the device and method of the instant claims *prima facie* obvious.

Response to Arguments

9. Applicant's arguments with respect to claims 1, 6, 7, 10, 11, 14, and 23-31 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

10. No claims allowed.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MY-CHAU T. TRAN whose telephone number is (571)272-0810. The examiner can normally be reached on Monday: 8:00-2:30; Tuesday-Thursday: 7:30-5:00; Friday: 8:00-3:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard A. Hjerpe can be reached on 571-272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/MY-CHAU T. TRAN/
Primary Examiner, Art Unit 2629

July 24, 2008